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(71) Applicant:
Matsushita Electric Industrial Co., Ltd.
Kadoma-shi, Osaka-fu, 571-8501 (JP)

(72) Inventors:
- Hamamoto, Yasuo
  Sakai-shi, Osaka 591-8004 (JP)
- Takeda, Hidetoshi
  Neyagawa-shi, Osaka 572-0089 (JP)

(74) Representative:
VOSSIUS & PARTNER
Siebertstrasse 4
81675 München (DE)

(54) Serial bus control apparatus

(57) Conventional serial bus of IEEE 1394 can not manage a transmission bandwidth and transmission channel for a future time. Therefore, it is not possible to make a reservation for recording from a STB to a VCR connected to the bus. The present invention makes it possible to perform a reservation management of the bus by defining and utilizing registers on CSR space for managing reservations of transmission bandwidth and transmission channel from present time to a future time.

In order to achieve the objects, a serial bus control apparatus of the present invention includes a means for providing a table for controlling a serial bus which has a function for securing a transmission bandwidth for the packet to the serial bus. The table is a reservation control table at least indicating a reservation of a transmission bandwidth and a transmission channel which is required from time T1 until time T2, the reservation control table is stored and controlled on a first register assigned to an address space which is accessible for reading and writing from an arbitrary node on the serial bus. The serial bus control apparatus of the present invention preferably includes a first detection part to detect that the present time is the time T1, the time T2, or the time between T1 and T2. Moreover, the serial bus control apparatus of the present invention preferably includes a rewriting part for rewriting a second register and a third register assigned to a particular address space for a particular node on the serial bus, which second register indicates the available transmission bandwidth at present time and which third register indicates the utilization status of the transmission channel at present time. The particular node on the serial bus is a node, which belongs to the serial bus control apparatus, and a node which includes the second register and the third register control apparatus of the present invention. The serial bus control apparatus of the present invention preferably includes a register providing part for providing a register for reservation control table which table is accessible for reading and writing from an arbitrary node of an arbitrary bus of the N piece of serial buses having the same standard time. In accordance with the present invention, a reservation management for future time using a serial bus for securing the transmission bandwidth and transmission channel according to IEEE 1394 can be achieved, which is not possible with conventional technology. Moreover the serial bus control apparatus of this invention is compatible with conventional systems.

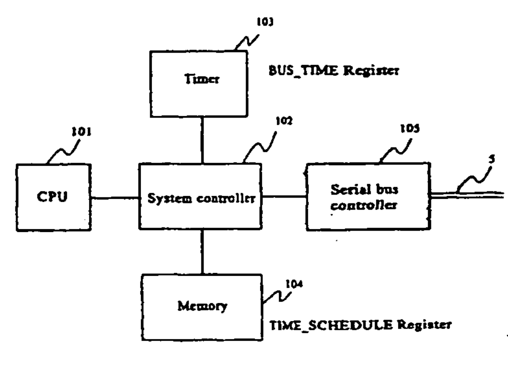

Fig. 1

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Description

[0001] The present invention relates to a serial bus control apparatus for controlling and performing a reservation of a transmission bandwidth and a transmission channel using the IEEE 1394 serial bus etc.

[0002] In recent years, two or more AVC equipment such as digital VCRs and personal computers are connected by using the ISO / IEC 13213 conforming serial bus such as IEEE 1394 serial buses, and a bandwidth secured transmission (isochronous transmission) of the video and the audio data is performed.

[0003] Figure 10 shows an example of the conventional method for performing a dubbing by a serial bus control apparatus when two digital VCRs generally used are connected each other by the IEEE 1394 serial bus. The isochronous transmission which uses IEEE 1394 is described in detail in the standard book "IEEE Standard for a High Performance Serial BUS" of IEEE Standard 1394 - 1995. One example of the conventional serial bus control apparatus above mentioned is described with reference to the drawing. Figure 10 shows the appearance of the dubbing in a digital VCR where a conventional serial bus control apparatus is installed. As shown in Figure 10, 1 denotes a first digital VCR, 2 denotes a second digital VCR, both VCRs are the nodes of the IEEE 1394 serial buses. 5 denotes the IEEE 1394 serial bus which connects both digital VCR 1 and 2 each other. When both nodes are connected each other by using IEEE 1394, an identification number, which is called physical-ID, is automatically allotted to each node respectively. In this case, the allotted ID number for the node of the first digital VCR is physical_ID = 0 and the allotted ID number for the node of the second digital VCR is physical_ID = 1. Data for which real time processing is required, such as video data or audio data etc., is transmitted in IEEE 1394 with a transmission system which secures the transmission band and the transmission channel, which is usually called isochronous transmission.

[0004] Figure 13 shows the appearance of the isochronous transmission. In the isochronous transmission, a node which is called a cycle muster (hereinafter, referred to as CM) performs a broadcast transmission of a cycle start packet 11 to the entire bus at 125 μsec cycles.

[0005] When the broadcast transmission of the cycle start packet is performed, the isochronous packet can be ready to transmit. At this time, a serial bus control apparatus which is called an isochronous resource manager (hereinafter, referred to as IRM) exists on the bus. To performs the isochronous transmission, it is necessary to declare securing the isochronous resource by using a register for securing the bandwidth (BANDWIDTH_AVAILABLE register) and a register for securing the channel (CHANNELS_AVAILABLE register) which IRM provides.

[0006] Figure 11 and Figure 12 show the bit allotment of the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register respectively. These registers are allotted in the CSR space defined by ISO / IEC 13213 as a serial bus dependent register. The BANDWIDTH_AVAILABLE register is a register of 32 bits (corresponding to 1 quadlet) as shown in Figure 11, the upper 19 bits are the reserved field, and lower 13 bits (bw_remaining) have significance. bw_remaining shows the isochronous bandwidth which can be allocated at the present time, and the initial value is 1001100110011b (corresponding to 4915d). The time to transmit and perform 1 quadlet with 1572.864 Mbps is defined as 1, and 125 μsec corresponds to 6144d. The time which can be allotted for the isochronous transmission is about 100 μsec, and it corresponds to a default value of 4915d. "b" fixed to the end of the figure indicates that the figure is the binary number and "d" indicates that the figure is the decimal number. It is necessary to rewrite the value of this register to start to perform the isochronous transmission. For instance, if 10 μsec of 125 μsec is required to be allotted to the isochronous transmission, 10 μsec corresponds to 492d, therefore, bandwidth is secured by rewriting the value of the register bw_remaining as 4423d (1000101000111b) (it is calculated as 4915d - 492d = 4423d).

[0007] Moreover, it is necessary to perform securing the transmission channel to perform the isochronous transmission. Securing the transmission channel is performed by using the CHANNELS_AVAILABLE register shown in Figure 12. This register is composed of 64 bits (corresponding to 2 quadlet), the upper 32 bits are defined as channels_available_hi and the lower 32 bits are defined as channels_available_lo. The isochronous channel of IEEE 1394, 64 of the 0th channel to the 63rd channels in total is available. The initial value of the CHANNELS_AVAILABLE register is 111111111111111111111111111111111111111111 1111111111111111111111b, and it indicates that all 64 channels are unused and available. For instance, in order to secure the first channel, the value of the CHANNELS_AVAILABLE register is rewritten as 111111111111111111111111111111111111111111 1111111111111111111101b. That is, each bit indicates the use of the channel of 0 to 63, and 1 is defined as used channel, 0 is defined as an unused channel.

[0008] In order to perform the isochronous transmission, the transmission bandwidth (corresponding to 125 μsec) and the transmission channel are secured by setting of the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register, then the cycle start packet is transmitted as shown in Figure 13(a), afterward the isochronous packet is transmitted after a gap time which is called an isochronous gap. In Figure 13(a), 12 indicates the period which is called a bus arbitration period, two or more nodes request the packet transmission to one bus at the same time, only one node can acquire the authority for the packet transmission. 13 indicates a period which is called a data prefix

period, or the period after which the packet is immediately transmitted. 14 indicates isochronous packet period, or the period for which the transmission data is transmitted. 15 indicates a period which is called the data end, it indicates that the transmission of the packet is ended. As shown in Figure 13(b), the period in which the isochronous packet can be transmitted is about 100 μsec after the cycle start, or the period for which the packet of two or more channels can be transmitted.

[0009] As shown in Figure 10, in this case, the second digital VCR is an IRM, the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register are available to IEEE 1394 serial bus 5. When the digital data of the first digital VCR is transmitted to the second digital VCR using the isochronous transmission, the data transmission (dubbing) is started after securing the transmission bandwidth and the transmission channel by the above-mentioned procedure. For instance, the first digital VCR and the second digital VCR are equipped with a physical layer which has the transmission ability of S100 (it is the transmission standard of 98.304 Mbps in the IEEE 1394). When the bandwidth of 40Mbps is transmitted by the channel 0, 40Mbps corresponds to 2500d, isochronous transmission is started with rewriting the value of bw_remaining as 0100101101111 (because 4915d-2500d = 2415d = 0100101101111), and the 0th bit of the channels_available_lo as 0b.

[0010] However, the above mentioned conventional serial bus control apparatus can only secure the current transmission bandwidth and the current transmission channel. There is no concept for time reservation of the transmission bandwidth and transmission channel. Therefore, when it is necessary to use the bus at certain period in future, it is not sure that the required transmission bandwidth and transmission channel is available or not.

[0011] Because of this, there are inconveniences in the serial bus control apparatus. For instance, when recording a program from the set top box connected with the bus to the digital VCR at certain time in the future with reservation by the timer, and if other nodes occupied the bus at the reserved time, the reserved recording by the timer can not be performed.

[0012] Therefore, with the foregoing in mind, it is an object of the present invention to provide a serial bus control apparatus for controlling the utilization of a bus, which can secure a transmission bandwidth and a channel of IEEE 1394 serial bus, at present time and future time.

[0013] In order to achieve the objects, a serial bus control apparatus of the present invention includes a means for providing a table for controlling a serial bus which has a function for securing a transmission bandwidth for the packet to the serial bus. The table is a reservation control table at least indicating a reservation of a transmission bandwidth and a transmission channel which is required from time T1 until time T2, the reservation control table is stored and controlled on a first register assigned to an address space which is accessible for reading and writing from an arbitrary node on the serial bus.

[0014] In one embodiment, the serial bus control apparatus of the present invention preferably includes a first detection part to detect that the present time is the time T1, the time T2, or the time between T1 and T2. Moreover, the serial bus control apparatus of the present invention preferably includes a rewriting part for rewriting a second register and a third register assigned to a particular address space for a particular node on the serial bus, which second register indicates the available transmission bandwidth at the present time and which third register indicates the utilization status of the transmission channel at the present time.

[0015] In one embodiment, the particular node on the serial bus is a node, which belongs to the serial bus control apparatus, and a node which includes the second register and the third register control apparatus of the present invention preferably includes the second and third registers.

[0016] In one embodiment, the serial bus control apparatus of the present invention preferably includes a register providing part for providing a register for reservation control table which table is accessible for reading and writing from an arbitrary node of an arbitrary bus of the N piece of serial buses having the same standard time.

[0017] In accordance with the present invention, A reservation management for future time using a serial bus for securing the transmission bandwidth and transmission channel according to IEEE 1394 can be achieved, which is not possible with conventional technology. Moreover, the serial bus control apparatus of this invention is compatible with conventional systems.

[0018] These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

Figure 1 is a block diagram showing a serial bus control apparatus of Embodiment 1 of this invention.

Figure 2 is a first bit field chart showing a TIME_SCHEDULE register of this invention.

Figure 3 is a bus block diagram of Embodiment 1 of this invention.

Figure 4 (a) is a reservation table of Embodiment 1 of this invention.

Figure 4 (b) is a bit field chart showing TIME_SCHEDULE register of Embodiment 1 of this invention.

Figure 5 is a register state transition diagram of Embodiment 1 of this invention.

Figure 6 is a block diagram showing a serial bus control apparatus of Embodiment 2 of this invention.

Figure 7 is a bus block diagram of Embodiment 2 of this invention.

Figure 8 (a) is a reservation table of Embodiment 2 of this invention.

Figure 8 (b) to (d) are bit field charts showing TIME_SCHEDULE registers of Embodiment 1 of this invention.

Figure 9 is a register state transition diagram of Embodiment 2 of this invention.

Figure 10 is a bus block diagram of the conventional technology.

Figure 11 is a bit field chart of showing BANDWIDTH_AVAILABLE register of IEEE 1394.

Figure 12 is a bit field chart of showing CHANNELS_AVAILABLE register of IEEE 1394.

Figure 13 (a) and (b) are a status charts showing an isochronous transmission of IEEE 1394.

Figure 14 is a bit field chart showing a BUS_TIME register of IEEE 1394.

Figure 15 is a second bit field chart showing a TIME_SCHEDULE register of this invention.

[0019] Hereinafter, the present invention will be described by way of embodiments with reference to the accompanying drawings.

(Embodiment 1)

[0020] Figure 1 shows a block diagram of a node which includes a first preferred example of a serial bus control apparatus of this invention.

[0021] In Figure 1, 101 denotes a CPU which controls a node. 102 denotes a system controller which includes an interface for the CPU 101, a memory 104, a timer 103 and a serial bus controller 105. 105 denotes a serial bus controller 105 for controlling data transmission of a serial bus of IEEE 1394. 5 denotes a serial bus of IEEE 1394. By this composition, a register which is called a TIME_SCHEDULE register is provided to the IEEE serial bus. The serial bus control apparatus of this invention is called as a Time Schedule Manager (hereinafter, referred to as TSM). The TSM composed as mentioned above can be built into personal computer 3 of Figure 3 for instance.

[0022] Figure 3 shows the bus composition which includes the node which has a serial bus controller (Time Schedule Manager, hereinafter referred to as TSM), of this invention.

[0023] 1 denotes a first digital VCR, 2 denotes a second digital VCR, 3 denotes a personal computer, 4 denotes a set top box (hereinafter, referred to as STB). It is assumed that the transmission ability of the physical layer is S100.

[0024] Physical_ID is allotted to each node based on the rule of IEEE1394. The physical_ID allotted to the first digital VCR 1 is 3 (physical_ID = 3), the physical_ID allotted to the second digital VCR 2 is 1 (physical_ID = 1), the physical_ID allotted to the personal computer 3 is 0 (physical_ID = 0), the physical_ID allotted to the first set top box 4 is 2 (physical_ID = 2).

[0025] In this example, the first digital VCR of physical_ID=3 performs as an IRM, and provides the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register to the IEEE 1394 serial bus. This node includes a CM function and performs the broadcast of the cycle start packet to the bus.

[0026] The TIME_SCHEDULE register is provided to the CSR space of the personal computer 3. The substance of the TIME_SCHEDULE register is the memory 104 shown in Figure 1. If there is a request for writing data to TIME_SCHEDULE register or reading data from the TIME_SCHEDULE register by the serial bus controller 105, the CPU 101 actually writes data to memory 104 or reads data from memory 104 and returns the result to the serial bus controller 105.

[0027] Figure 2 shows an example of the bit allotment of the TIME_SCHEDULE register. The register of three quadlet is defined corresponding to one tune schedules. The # 0 to the # M TIME_SCHEDULE register (M is an integer of 0 or more) is defined in the continuous address to control two or more time schedule.

[0028] In the TIME_SCHEDULE register, the upper seven bits of the quadlet are not used. The following six bits are physical_ID of the node which preserves the time schedule. The following six bits indicate the channel number which is reserved and performed with request_channel_number. The following 13 bits indicate the bandwidth to be reserved by request_bw.

[0029] The second quadlet indicates the time when the reservation is started and performed. According to the definition of the BUS_TIME register of IEEE 1394, the upper 25 bits are defined as the start_second_count_hi and the lower 7 bits are defined as start_second_count_lo.

[0030] The third quadlet indicate the time when the reservation is ended and performed. According to the definition of the BUS_TIME register of IEEE 1394, the upper 25 bits are defined as the start_second_count_hi and the lower 7 bits are defined as start_second_count_lo.

[0031] Figure 14 shows the BUS_TIME register of the serial bus of IEEE 1394. It is a counter of 32 bits which counts by second and can count 136 years of time. In the above description, the 32 bits are separated into second_count_hi and second_count_lo. However, the separation has no special meaning in this Embodiment 1.

[0032] The initial value of the TIME_SCEDULE register is request_bw = 000000000000b. Other bits can take any value. As a result, The ID number of the TIME_SCHEDULE register which is used for the time reservation can be detected.

[0033] As shown in Figure 4 (a), in order to operate the reserved recording from the first set top box shown in Figure 3 to the first digital VCR from 6 o'clock to 18 o'clock on October 10, when the personal computer

reserves 25 Mbps bandwidth by channel 1, the bit assignment are that

physical_ID = 000000b,
request_channel_number = 000001b,
request_bw = 0011000100000b,
start_second_count_hi = 0000000000000000010101000b,
start_second_count_lo = 1100000b,
end_second_count_hi = 0000000000000000111111010b,
start_second_count_lo = 0100000b.

[0034] This value is written in the TIME_SCHEDULE register. To simplify explanation, in the BUS_TIME, 0 o'clock of October 10 is set to as 0.

[0035] Moreover, this reservation is set to the # 0 TIME_SCHEDULE register and assigned bit in other register is request_bw=0000000000000b. Therefore, other time reservation is not set.

[0036] Moreover, before reservation, the node performing reservation reads out all TIME_SCHEDULE registers and confirms that necessary bandwidth and channel are available or not at the time to be reserved. If necessary bandwidth and channel are available at the time to be reserved, the reserved recording can be set.

[0037] Figure 5 shows the change in the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register of IRM of the reservation mentioned above.

[0038] The values of these registers for between 0 o'clock and 6 o'clock on October 10 are the initial values. In this Embodiment 1, the channels_available_hi which is the upper 32 bits of the CHANNELS_AVAILABLE register is not described because it has not been changed from the initial value. The bandwidth of 25Mbps is used by channel 1 for between 6 o'clock and 18 o'clock on October 10, the isochronous transmission is started with rewriting the bw_remaining as (1001100110011b - 0011000100000b =) 0110100011001 1b, and the channels_available_lo as 11111111111111111111111111111101b. Rewriting of these two registers can be performed by any node on the bus. It is not necessary that the node of physical_ID = 000000b performs the rewriting.

[0039] After 18 o'clock on October 10, the bus is used. Therefore, the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register are returned to the initial value. When the reserved time is over, request_bw of the corresponding TIME_SCHEDULE register should be reserved to 0000000000000b.

[0040] According to the above mentioned preferred Embodiment 1, the serial bus control apparatus of this invention includes a BANDWIDTH_AVAILABLE register and a CHANNELS_AVAILABLE register controlled by the IRM as well as TIME_SCHEDLUE register of the TSM of the present invention. The serial bus control apparatus controls the reservation information regarding time schedule by the TIME_SCHEDLUE register and secures the isochronous bandwidth and isochronous channel using the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register at the time to be reserved.

[0041] According to this operation, the reservation management for future time can be achieved, which is not possible by the conventional technology. Moreover, the serial bus control apparatus of this invention is compatible with conventional systems.

(Embodiment 2)

[0042] Hereinafter, Embodiment 2 of the present invention will be described with reference to the accompanying drawings.

[0043] Figure 6 shows a block diagram of a serial bus bridge as a serial bus control apparatus including plural of serial buses having the TSM of Embodiment 2 of this invention. In Figure 6, 101 denotes CPU, which controls a node. 102 denotes a system controller which includes an interface for the CPU 101, a memory 104, a timer 103 and a serial bus controller 105, 106 and 107. Each 105 to 107 denotes a serial bus controller for controlling data transmission of a serial bus of IEEE 1394. 5 denotes a serial bus of IEEE 1394. By this composition, a register which is called a TIME_SCHEDULE register is provided to the IEEE serial bus. Normally, it is better that the bus bridge acts as IRM for each bus. Therefore, the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register to be provided to each bus are equipped. Two or more buses are connected and perform using the above described bus bridge in which TMS is equipped.

[0044] Figure 7 shows the bus composition which includes the plural bus connected via bus bridge having the serial bus controller (TSM) of this invention. 1 denotes a first digital VCR, 2 denotes a second digital VCR, 3 denotes a personal computer, 7 denotes a first digital television set (hereinafter, referred to as TV). These nodes are connected to the serial bus whose BUS_ID is 0 (BUS_ID = 0), and connected to the bus bridge 10. 6 denotes a third digital VCR and 4 denotes a first STB. These nodes are connected to the serial bus whose BUS_ID is 1 (BUS_ID = 1), and connected to the bus bridge 10. 8 denotes a second STB, and 9 denotes a printer. These nodes are connected to the serial bus whose BUS_ID is 2, and connected with bus bridge 10. It is assumed that the transmission ability of the physical layer of each bus is S100.

[0045] Physical_ID is allotted to each node of buses based on the rule of IEEE1394. Regarding the BUS_ID = 0, the physical_ID allotted to the first digital VCR 1 is 3 (physical_ID = 3), the physical_ID allotted to the second digital VCR 2 is 1 (physical_ID = 1), the physical_ID allotted to the personal computer 3 is 0 (physical_ID = 0), the physical_ID allotted to the bus bridge 10 is 4 (physical_ID = 4). Regarding the BUS_ID = 1, the

physical_ID allotted to the third digital VC 1 is 1 (physical_ID = 1), the physical_ID allotted to the first STB 4 is 0 (physical_ID = 0), the physical_ID allotted to the bus bridge 10 is 2 (physical_ID = 2). Regarding the BUS_ID = 2, the physical_ID allotted to the second STB 8 is 1 (physical_ID = 1), the physical_ID allotted to the printer 9 is 0 (physical_ID = 0), the physical_ID allotted to the bus bridge 10 is 2 (physical_ID = 2).

[0046] In this example, the bus bridge 10 becomes CM, IRM, and TSM in order to achieve the cycle synchronization of each bus and to control the plural buses efficiently. That is, synchronization is taken respectively for each bus, the cycle start packet is broadcasted, and the independent BANDWIDTH_AVAILABLE register, CHANNELS_AVAILABLE register and TIME_SCHEDULE register are provided to each bus. The substance of each register provided to each bus is a memory 104 shown in Figure 6. If there is a request for writing data to each register or reading data from each register by the serial bus controller 105 ~ 107, the CPU 101 actually writes data to memory 104 or reads data from memory 104 and returns the result to the serial bus controller 105 ~ 107.

[0047] An example of the bit allotment for each register can be the same as Embodiment 1.

[0048] As shown in Figure 8 (a), in order to operate the reserved recording from the first set top box shown in Figure 6 to the third digital VCR from 6 o'clock to 18 o'clock on October 10, when the first STB reserves 25 Mbps bandwidth by channel 0, data transmission is performed on the bus whose BUS_ID is 0 (BUS_ID = 0), data is written in the TIME_SCHEDULE register of the TSM # 1 of the BUS_ID = 1.

[0049] In this case, as shown in Figure 8 (c) #0, the bit assignments are that

physical_ID = 000000b,
request_channel_number = 000000b,
request_bw = 0011000100000b,
start_second_count_hi = 000000000000000010101000b,
start_second_count_lo = 1100000b,

end_second_count_hi=00000000000000001111 1010b,
start_second_count_lo = 0100000b.

These values are written in the TIME_SCHEDULE register of TSM #1. The same as Embodiment 1, to simplify the explanation, in the BUS_TIME, 0 o'clock of October 10 is set to 0.

[0050] Next, According to Figure 8(a), the recording reservation is performed from the second STB shown in Figure 6 to the first digital VCR from 12 o'clock to 24 o'clock on October 10. The second STB is a node of the bus whose BUS_ID = 2, and the first digital VCR is a node of the bus whose BUS_ID = 0. Therefore, data is transmitted over two buses. Therefore, data is written in the TIME_SCHEDULE register of each TMS of BUS_ID=2 and BUS_ID=0. In this case, reservation to each bus with transmission bandwidth 50Mbps and channel 0 is set.

[0051] It is possible to set reservation using channel 0 of the bus whose BUS_ID=0 and BUS_ID=2 which are available from 12 o'clock to 18 o'clock though the channel 0 of the bus whose BUS_ID=1 has already been used. In this case, data are written in # 0 of the table (d) and # 0 of the table (d) shown in Figure 8.

[0052] When the second STB makes the reservation, the value of the TIME_SCHEDULE register of the TSM # 2 will be rewritten in order to reserve the bus whose BUS_ID is 2. The bit assignments are that

physical_ID = 000001b,
request_channel_number=000000b,
request_bw=0110001000000b,

start_second_count_hi=000000000000000010101 0001b,
start_second_count_lo=1000000b,

end_second_count_hi=000000000000000101010 0011b,
start_second_count_lo=0000000b.

[0053] The value of the TIME_SCHEDULE register of the TSM # 0 will be rewritten in order to reserve the bus whose BUS_ID is 0. The bit assignments are that

physical_ID = 000100b,
request_channel_number = 000000,
request_bw = 0110001000000b,
start_second-count_hi = 0000000000000000101010001b,
start_second_count_lo = 1000000b,
end_second_count_hi = 0000000000000001010100011b,
start_second_count_lo = 0000000b.

[0054] In this case, because the node of another bus has made reservation to TSM #0 through the bridge, the physical_ID of the bridge of BUS_ID=0 is written to the bit field for physical_ID. In this case, physical_ID=000100b.

[0055] In addition, according to Figure 8(a), the recording reservation from the first STB shown in Figure 6 to the second digital VCR is performed from 12 o'clock October 10 to 6 o'clock October 11. In this case, data are transmitted over the bus of which BUS_ID=1 and the bus of which BUS_ID = 0. Because channel 0 has already been reserved by both bus whose BUS_ID=1 and bus whose-BUS_ID=0, it is necessary to reserve other channels. In the above description, channel 1 is selected as a reserved channel because channel 1 in both the bus whose BUS_ID=0 and the bus whose BUS_ID=1 is available, another channel can be

selected if it is available in both buses.

[0056] In this case, # 1 in Figure 8(c) and # 1 in Figure 8(b) are selected for writing. The register for the TIME_SCHEDULE register can be selected from unused available registers (register whose request_bw = 0000000000000b). In the above description, register # 1 is selected.

[0057] When the first STB makes the reservation, the value of the TIME_SCHEDULE register of the TSM # 1 will be rewritten in order to reserve the bus whose BUS_ID is 1. The bit assignments are that

physical_ID = 000000b,
request_channel_number = 000001b,
request_bw=0000010111100b,
start_second_count_hi = 0000000000000000101010001b,
start_second_count_lo = 1000000b,
end_second_count_hi = 0000000000000001101001011b,
start_second_count_lo = 1100000b.

[0058] The value of the TIME_SCHEDULE register of the TSM # 0 will be rewritten in order to reserve the bus whose BUS_ID = 0. The bit assignments are that

physical_ID = 000100b,
request_channel_number = 000001b,
request_bw = 0000010111100b,
start_second_count_hi = 0000000000000000101010001b,
start_second_count_lo = 1000000b,
end_second_count_hi = 0000000000000001101001011b,
start_second_count_lo = 1100000b.

[0059] In this case, because the node of another bus has made reservation to TSM #0 through the bridge, the physical_ID of the bridge of BUS_ID=0 is written to the bit field for physical_ID. In this case, physical_ID=000100b.

[0060] The same as Embodiment 1, when a node makes reservation, the node reads out values of all TIME_SCHEDULE register of buses for reserving the bandwidth and confirms whether the necessary bandwidth and necessary channel remains or not. When the necessary bandwidth and necessary channel remains, the node can make reservation. Thus, three kinds of reservations shown in Figure 8(a) are performed completely.

[0061] Figure 9 shows the change in the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register of IRM #0 to #2 by the above mentioned reservation. The value of these registers between from 0 o'clock to 6 o'clock on October 10 remains as the initial values. In this Embodiment 2, because the channels_available_hi which is the upper 32 bits of the CHANNELS_AVAILABLE register has not been changed and remains as initial value, it is not described.

[0062] In the bus whose BUS_ID = 1, the bandwidth of 25Mbps is used by channel 0 between from 6 o'clock to 18 o'clock on October 10, the isochronous transmission is started with rewriting the bw_remaining as

(1001100110011b - 0011000100000b =) 0110100010011b, and
the channels_available_lo as 11111111111111111111111111111110b.

Rewriting of this two register can be performed by any node on the bus. It is not necessary that the node of physical_ID = 000000b performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0063] Between from 12 o'clock to 18 o'clock on October 10, in order to use 50Mbps bandwidth by channel 0 between the bus whose BUS_ID = 2 and the bus whose BUS_ID = 0, and to use 3Mbps bandwidth by channel 1 between the bus whose BUS_ID = 1 and the bus whose BUS_ID = 0, the isochronous transmission is started with rewriting the register of the IRM #0 as

bw_remaining = 1001100110011b-0110001000000b-0000010111100b = 0011000110111b,
channels_available_lo = 11111111111111111111111111111100b,
rewriting the register of the IRM #1 as
bw_remaining = 0110100010011b-0000010111100b = 0110001010111b,
channels_available_lo = 11111111111111111111111111111100b,
rewriting the register of the IRM #2 as
bw_remaining = 1001100110011b-0110001000000b = 0011011110011b,
channels_available_lo = 11111111111111111111111111111110b.

Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0064] Between 18 o'clock to 24 o'clock on October 10, the recording from the first STB to the third digital VCR performed on the bus whose BUS_ID = 1 is finished. At this time, it is necessary to release channel 0 which was used for 25Mbps bandwidth transmission. Therefore, the bit field of the register of the IRM #1

should be rewritten as

the bw_remaining = 0110001010111b + 0011000100000b = 1001001110111b, channels_available_lo = 11111111111111111111111111111101b.

Moreover, because the reservation time ended, it is necessary to release the TIME_SCHEDULE register of TSM #1. Because this was written in Figure 8(c) #0, the request_bw should be rewritten as 0000000000000b in order to enable other nodes to use this register. Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0065] Between 0 o'clock to 6 o'clock on October 11, the recording from the second STB to the first digital VCR performed between the bus whose BUS_ID = 2 and the bus whose BUS_ID = 0 is finished. At this time, it is necessary to release channel 0 which was used for 50Mbps bandwidth transmission. Therefore, the bit field of the IRM #0 should be rewritten as

bw_remaining = 0011000110111b + 0110001000000b = 1001001110111b, channels_available_lo = 11111111111111111111111111111101b,
the bit field of the IRM #2 should be rewritten as the bw_remaining = 0011011110011b + 0110001000000b = 1001100110011b,

channels_available_lo=1111111111111111111111 1111111111b.

Moreover, because the reservation time ended, it is necessary to release the TIME_SCHEDULE register of TSM #2 and TSM #0. Because this was written in Figure 8(d) #0 and Figure 8(b) #0, the request_bw should be rewritten as 0000000000000b in order to enable other nodes to use this register. Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0066] After 6 o'clock on October 11, the recording from the first STB to the second digital VCR performed between the bus whose BUS_ID = 1 and the bus whose BUS_ID = 0 is finished. At this time, it is necessary to release channel 1 which was used for 3Mbps bandwidth transmission. Therefore, the bit field of the IRM #0 should be rewritten as the bw_remaining = 1001001110111b + 0000010111100b = 1001100110011b, channels_available_lo = 11111111111111111111111111111111b, the bit field of the IRM #1 should be rewritten as

bw_remaining = 1001001110111b + 0000010111100b = 1001100110011b, channels_available_lo = 11111111111111111111111111111111b.

Moreover, because the reservation time ended, it is necessary to release the TIME_SCHEDULE register of TSM #1 and TSM #0. Because this was written in Figure 8(c) #0 and Figure 8(b) #0, the request_bw should be rewritten as 0000000000000b in order to enable other nodes to use this register. Rewriting of these registers can be performed by any node on the bus. It is not necessary that the node which had made reservation performs the rewriting. Moreover, because the bus bridge is a node which has both the function of TSM and IRM, the node can perform register bit field rewriting automatically by detecting the reserved time arrival by CPU 101 with the built in clock 103.

[0067] According to the above mentioned preferred Embodiment 2, the serial bus control apparatus of this invention includes BANDWIDTH_AVAILABLE registers and CHANNELS_AVAILABLE registers controlled by the IRM as well as TIME_SCHEDLUE register of the TSM of the present invention. The serial bus control apparatus controls the reservation information regarding time schedule by the TIME_SCHEDLUE register and secures the isochronous bandwidth and isochronous channel using the BANDWIDTH_AVAILABLE register and the CHANNELS_AVAILABLE register at the time to be reserved.

[0068] According to this operation, the reservation management for future time can be achieved, which is not possible with conventional technology. Moreover, the serial bus control apparatus of this invention is compatible with conventional systems. The TIME_SCHEDULE register of this Embodiment does not prepare the bit for describing BUS_ID of the node which made reservation, BUS_ID can be added as shown in Figure 15 in order to control.

[0069] In the case where a conventional node, which does not correspond to the TSM of the present invention, is connected to the bus of the present invention, there are problems in that the conventional node reserves the transmission bandwidth and the transmission channel for IRM without reservation registration in the TIME_SCHEDULE register and starts the isochronous packet transmission. Another problem is that the conventional node releases the transmission bandwidth and the transmission channel for IRM without canceling the reservation for the TIME_SCHEDULE register.

[0070] In order to prevent these problems, it is neces-

sary to prohibit the conventional node to access the IRM and TSM. These problems will be solved if the node which corresponds to TSM of this invention performs the reservation and cancellation for bandwidth and channel to IRM and TSM, and the conventional node performs the actual isochronous packet transmission. However, in the case that the conventional node, which does not know the existence of the TSM of the present invention, performs the access for IRM independently and transmits isochronous packet without registration to TSM, for example, in Figure 8(a), the 40 Mbps isochronous transmission from the first conventional node to the second conventional node without registering TSM, it is impossible to start the reserved 50 Mbps transmission from 12 o'clock on October 10 because of available bandwidth overflow. In this case, the operation of the conventional node should be stopped for stopping the 40 Mbps transmission in order to recover the status of the system as the normal status.

[0071] It is also possible to solve the problems by stopping the reserved 50 Mbps transmission from 12 o'clock.

[0072] What measures should be taken for these problems is selected by system application with consideration of the priority and the appropriate countermeasure that should be performed.

[0073] Moreover, the serial bus of IEEE 1394 is used in the above described Embodiment, other buses are acceptable if that can perform transmission by which the transmission bandwidth is secured.

[0074] The invention may be embodied in other forms without departing from the spirit or essential characteristics thereof. The embodiments disclosed in this application are to be considered in all respects as illustrative and not limitative, the scope of the invention is indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

Claims

1. A serial bus control apparatus comprising:

   a means for providing a table for controlling a serial bus which has a function for securing a transmission bandwidth for a packet to the serial bus;
   wherein the table is a reservation control table at least indicating a reservation of a transmission bandwidth and a transmission channel which is required from time T1 until time T2, the reservation control table is stored and controlled on a first register assigned to an address space which is accessible for reading and writing from an arbitrary node on the serial bus.

2. The serial bus control apparatus according to claim 1, further comprising a first detection part to detect that a present time is the time T1, the time T2, or time between T1 and T2, a rewriting part for rewriting a second register and a third register assigned to a particular address space for a particular node on the serial bus, which second register indicates available transmission bandwidth at present time and which third register indicates utilization status of the transmission channel at present time.

3. The serial bus control apparatus according to claim 2 wherein

   the particular node on the serial bus is a node, which belongs to the serial bus control apparatus, and a node which includes the second register and the third register.

4. The serial bus control apparatus according to any one of claims 1 to 3, further comprising a register providing part for providing a register for reservation control table which table is accessible for reading and writing from an arbitrary node of an arbitrary bus of an N piece of serial buses having a same standard time.

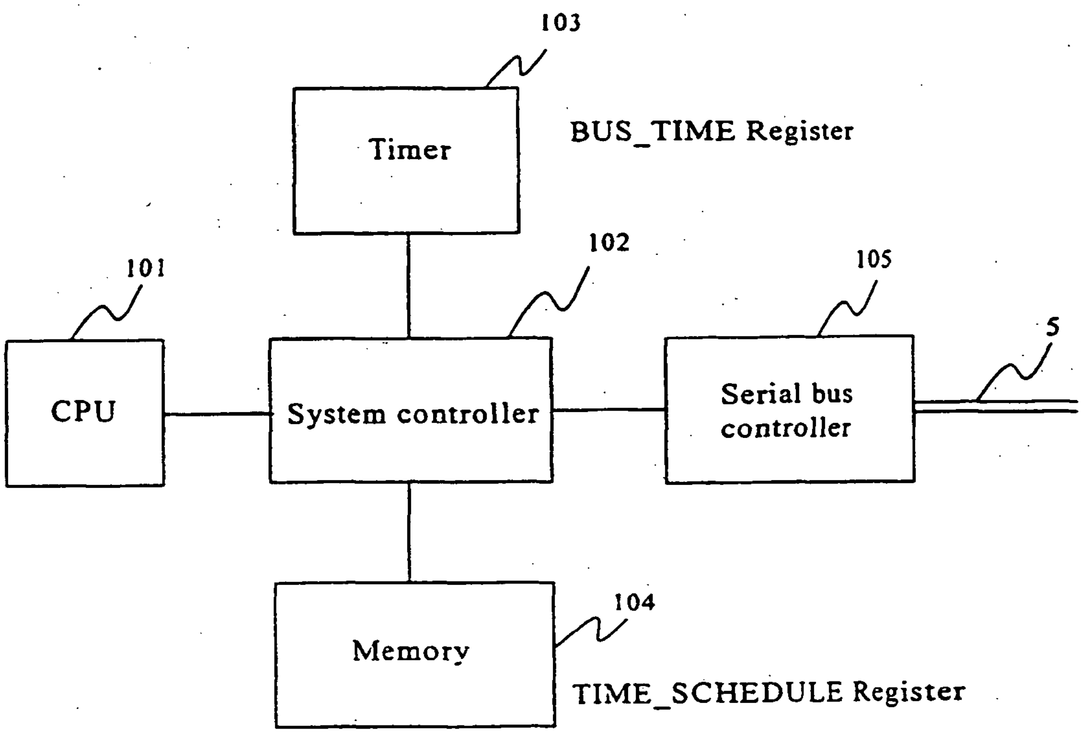

103
Timer
BUS_TIME Register
102
101
105
5
CPU
System controller
Serial bus
controller
104
Memory
TIME_SCHEDULE Register

Fig. 1

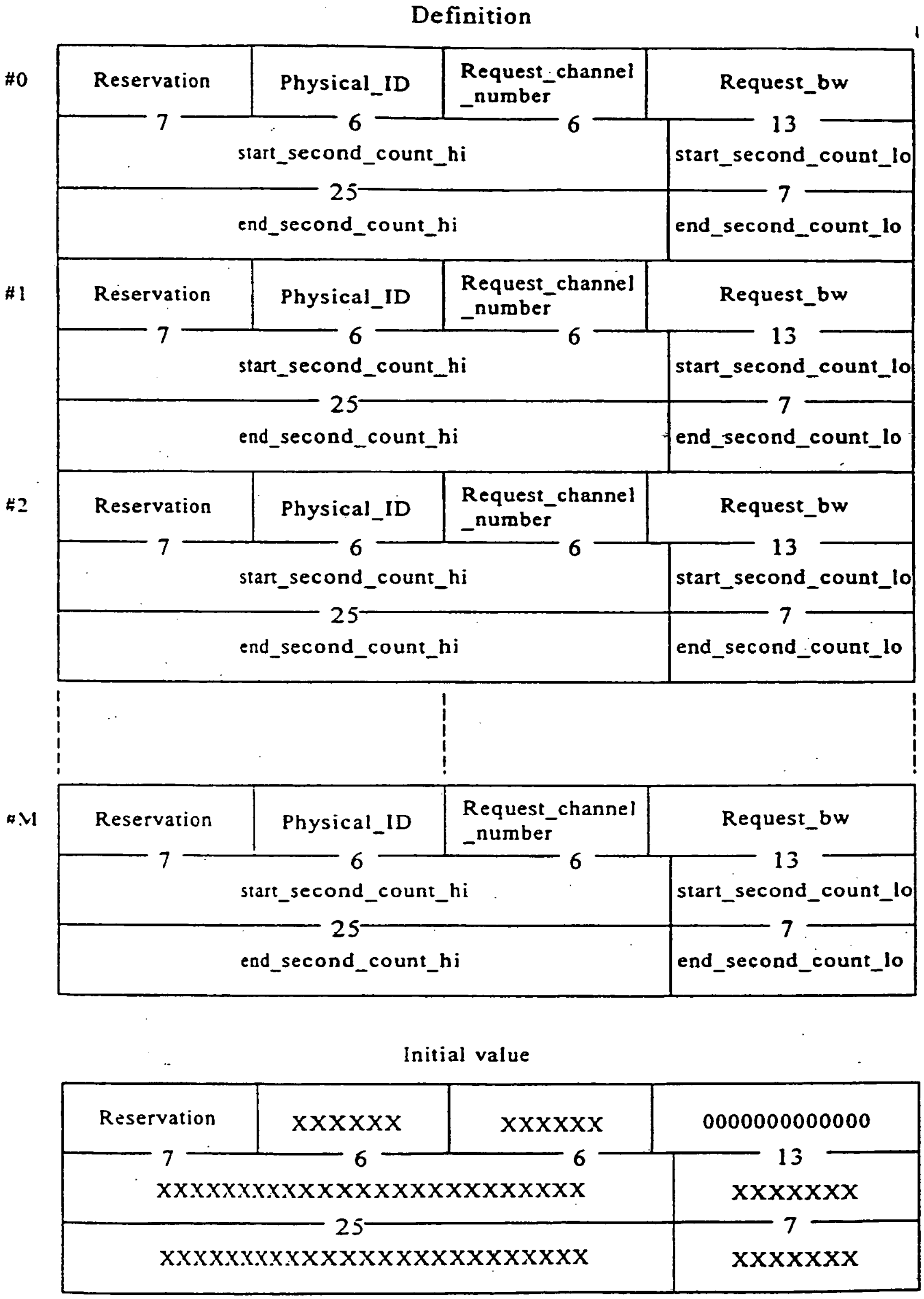

Definition
#0
Reservation
Physical_ID
Request_channel _number
Request_bw
7
6
6
13
start_second_count_hi
start_second_count_lo
25
7
end_second_count_hi
end_second_count_lo
#1
Reservation
Physical_ID
Request_channel _number
Request_bw
7
6
6
13
start_second_count_hi
start_second_count_lo
25
7
end_second_count_hi
end_second_count_lo
#2
Reservation
Physical_ID
Request_channel _number
Request_bw
7
6
6
13
start_second_count_hi
start_second_count_lo
25
7
end_second_count_hi
end_second_count_lo
#M
Reservation
Physical_ID
Request_channel _number
Request_bw
7
6
6
13
start_second_count_hi
start_second_count_lo
25
7
end_second_count_hi
end_second_count_lo
Initial value
Reservation
XXXXXX
XXXXXX
0000000000000
7
6
6
13
XXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXX
25
7
XXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXX

Fig. 2

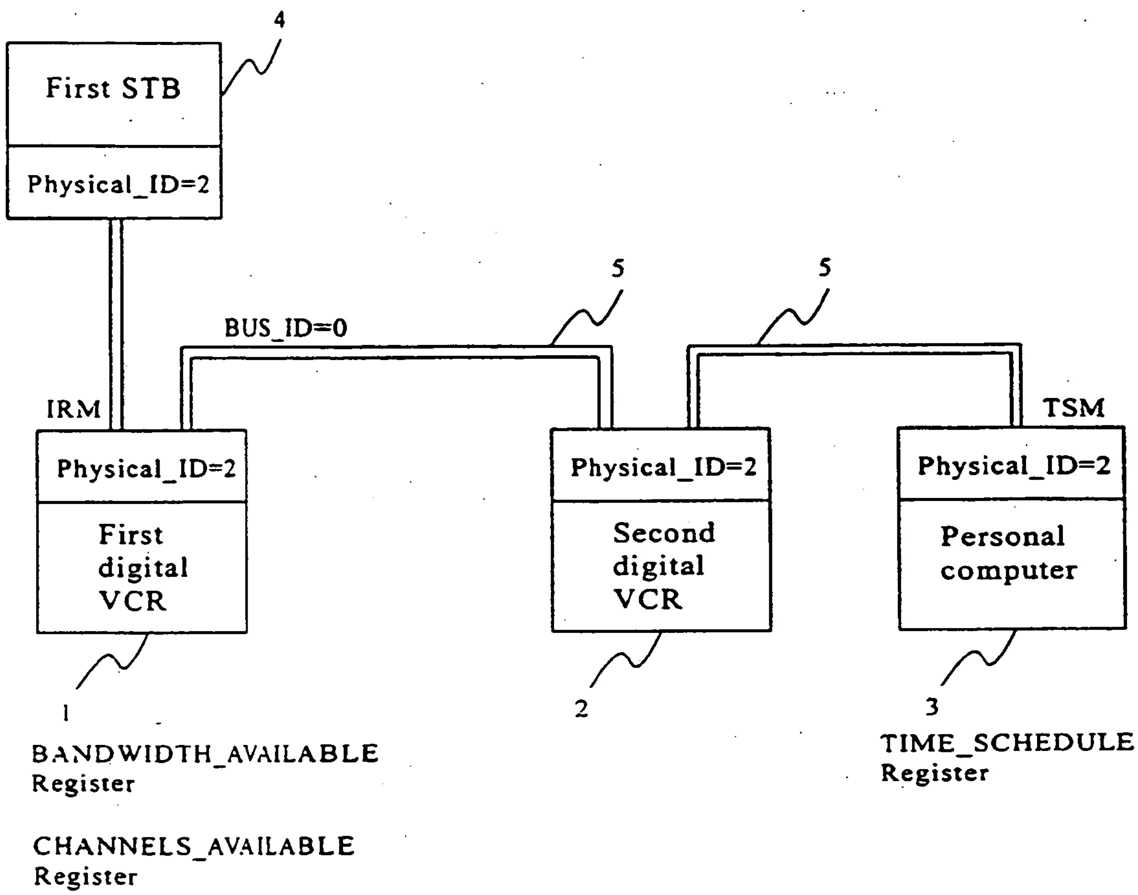

4
First STB
Physical_ID=2
5
5
BUS_ID=0
IRM
TSM
Physical_ID=2
First digital VCR
Physical_ID=2
Second digital VCR
Physical_ID=2
Personal computer
1
2
3
BANDWIDTH_AVAILABLE Register
CHANNELS_AVAILABLE Register
TIME_SCHEDULE Register

Fig. 3

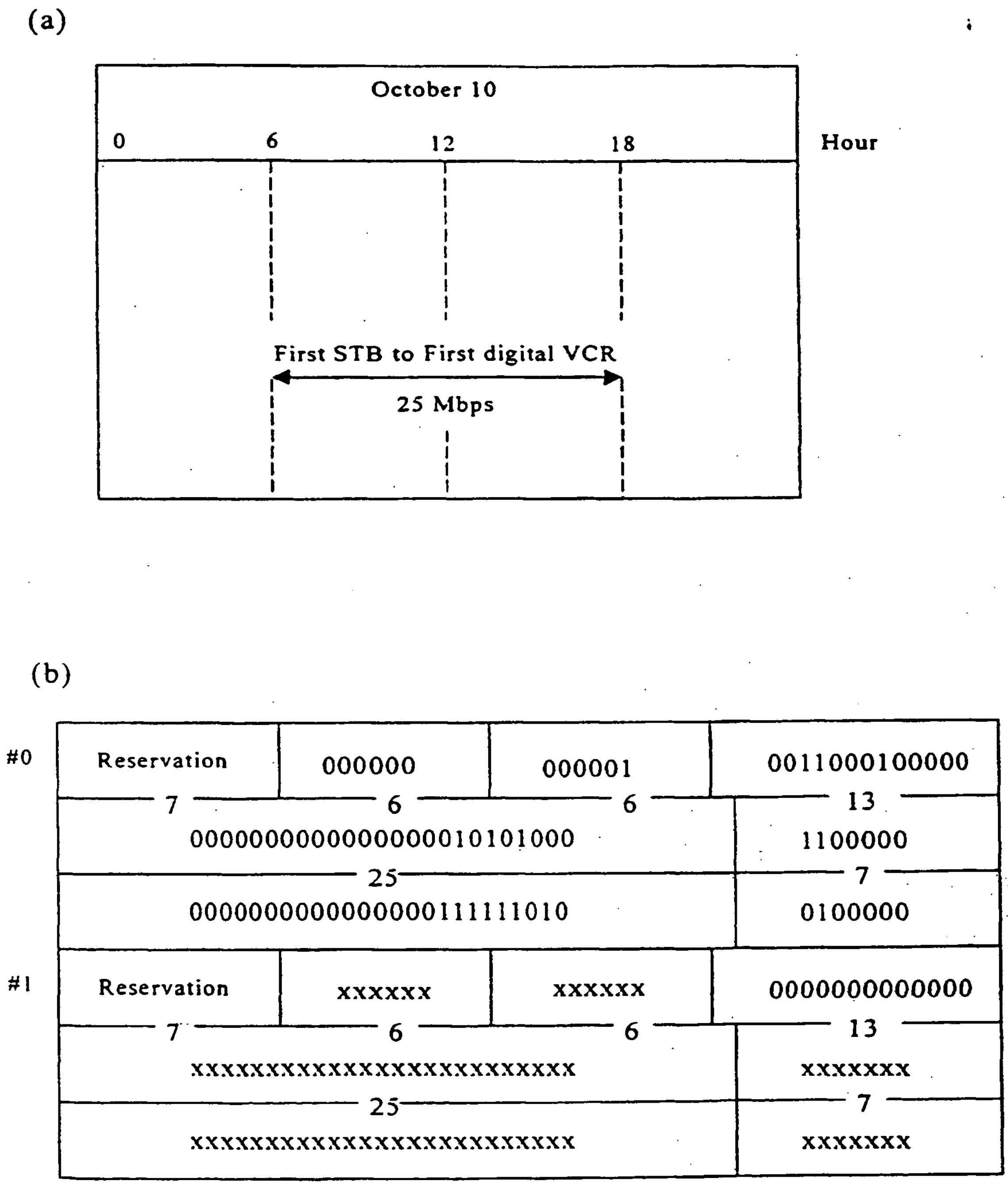

(a)
October 10
0
6
12
18
Hour
First STB to First digital VCR
25 Mbps
(b)
#0
Reservation
000000
000001
0011000100000
7
6
6
13
0000000000000000010101000
1100000
25
7
0000000000000000111111010
0100000
#1
Reservation
xxxxxx
xxxxxx
0000000000000
7
6
6
13
xxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxx
25
7
xxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxx

Fig. 4

October 10 0 o'clock | 6 o'clock	BANDWIDTH_AVAILABLE bw_remaining	1001100110011
	channel_available_lo	1111111111111111 1111111111111111
October 10 6 o'clock | 18 o'clock	BANDWIDTH_AVAILABLE bw_remaining	0110100010011
	channel_available_lo	1111111111111111 1111111111111101
October 10 18 o'clock | 24 o'clock	BANDWIDTH_AVAILABLE bw_remaining	1001100110011
	channel_available_lo	1111111111111111 1111111111111111

Fig. 5

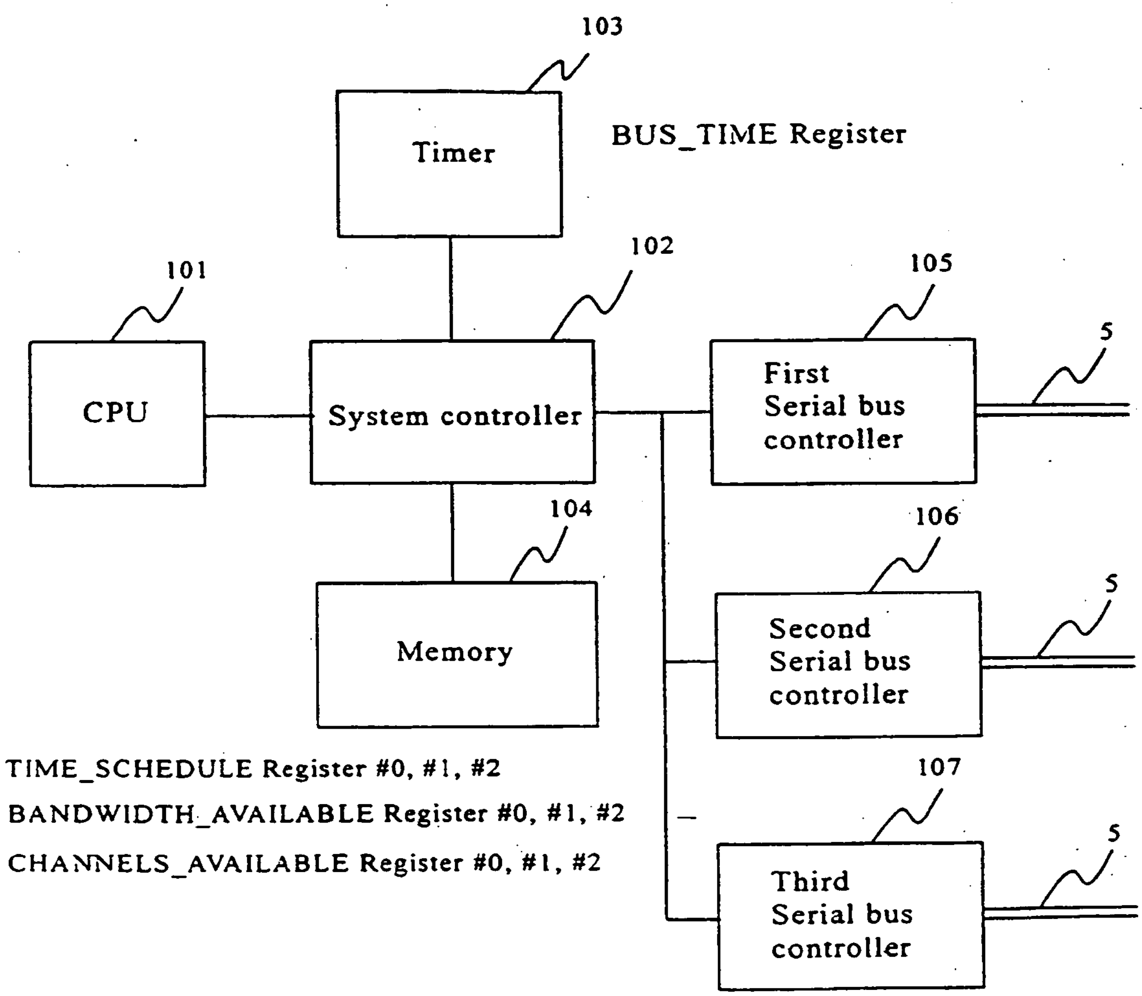
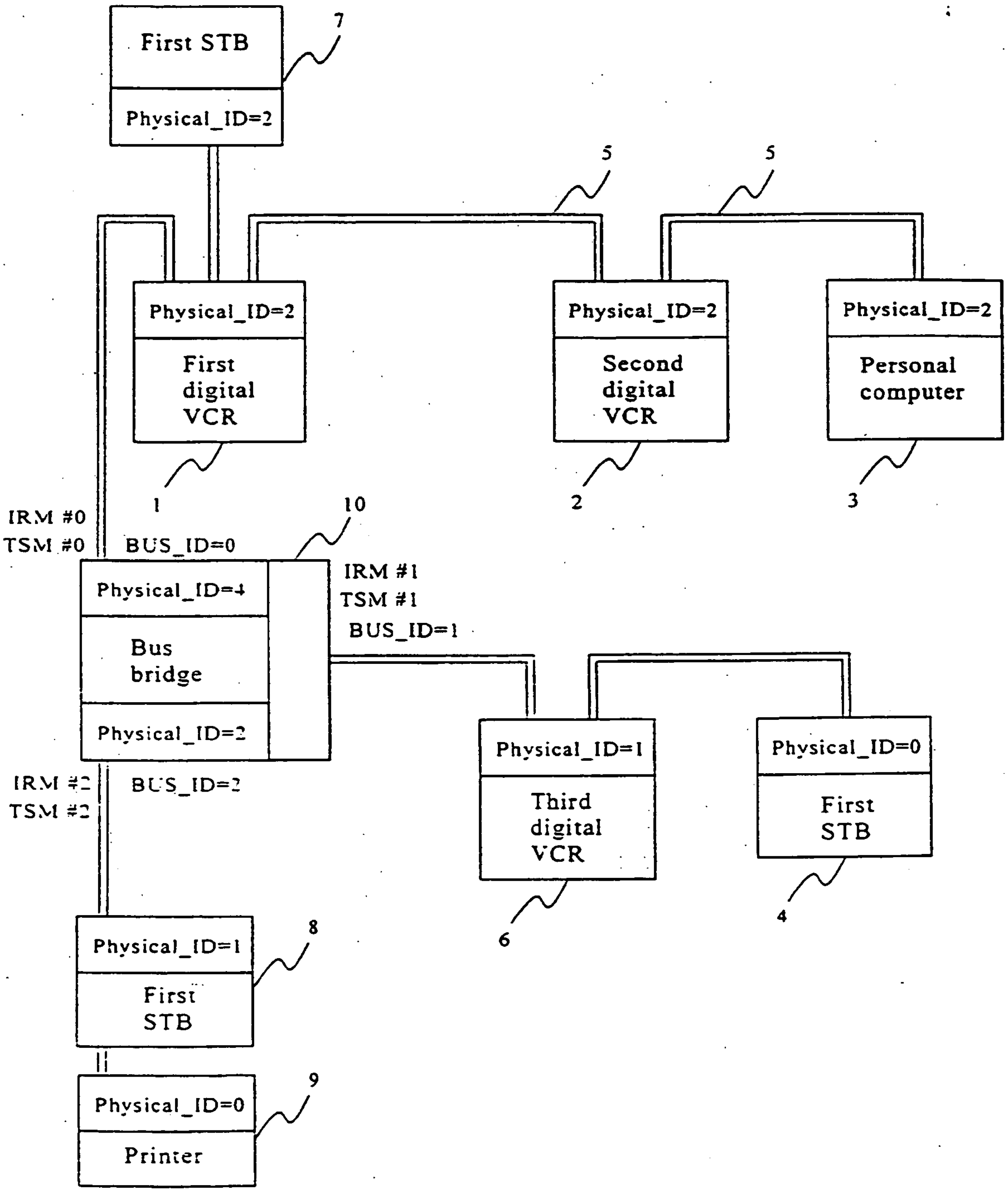

103
Timer
BUS_TIME Register
101
CPU
102
System controller
105
First Serial bus controller
5
104
Memory
106
Second Serial bus controller
5
107
Third Serial bus controller
5
TIME_SCHEDULE Register #0, #1, #2
BANDWIDTH_AVAILABLE Register #0, #1, #2
CHANNELS_AVAILABLE Register #0, #1, #2

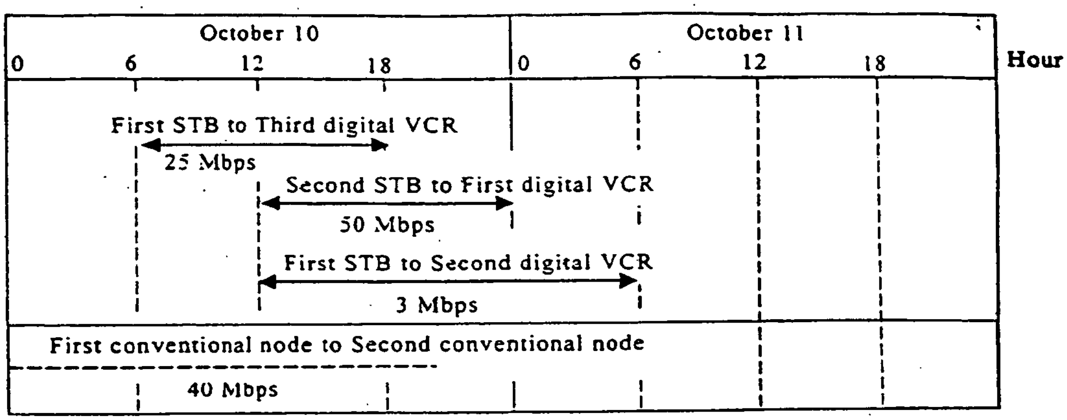
Fig. 6



First STB
Physical_ID=2
7
5
5
Physical_ID=2
First digital VCR
Physical_ID=2
Second digital VCR
Physical_ID=2
Personal computer
1
2
3
10
IRM #0
TSM #0
BUS_ID=0
Physical_ID=4
Bus bridge
Physical_ID=2
IRM #1
TSM #1
BUS_ID=1
IRM #2
TSM #2
BUS_ID=2
Physical_ID=1
Third digital VCR
Physical_ID=0
First STB
6
4
Physical_ID=1
First STB
8
Physical_ID=0
Printer
9

Fig. 7

(a)



(b) BUS_ID=0

TSM #0

#0	Reservation	000100	000000	0011000100000
	0000000000000000101010001			1100000
	0000000000000000101010011			0000000
#1	Reservation	000100	000001	0000010111100
	0000000000000000101010001			1100000
	0000000000000001101001011			1100000
#2	Reservation	xxxxxx	xxxxxx	0000000000000
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx

(c) BUS_ID=1

TSM #1

#0	Reservation	000000	000000	001100010000
	0000000000000000101010000			1100000
	0000000000000000111111010			0100000
#1	Reservation	000000	000001	0000010111100
	0000000000000000101010001			1000000
	0000000000000001101001011			1100000
#2	Reservation	xxxxxx	xxxxxx	0000000000000
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx

(d) BUS_ID=2

TSM #2

#0	Reservation	000001	000000	0110001000000
	0000000000000000101010001			1000000
	0000000000000000101010011			0000000
#1	Reservation	xxxxxx	xxxxxx	0000000000000
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx
#2	Reservation	xxxxxx	xxxxxx	0000000000000
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx
	xxxxxxxxxxxxxxxxxxxxxxxxx			xxxxxxx

Fig. 8

		BUS_ID=0 IRM #0	BUS_ID=1 IRM #1	BUS_ID=2 IRM #2
October 10 0-6 o'clock	BANDWIDTH_AVAILABLE Bw_remaining	1001100110011	1001100110011	1001100110011
	Channels_available_lo	1111111111111111 1111111111111111	1111111111111111 1111111111111111	1111111111111111 1111111111111111
October 10 6-12 o'clock	BANDWIDTH_AVAILABLE Bw_remaining	1001100110011	0110100010011	1001100110011
	Channels_available_lo	1111111111111111 1111111111111111	1111111111111111 1111111111111110	1111111111111111 1111111111111111
October 10 12-18 o'clock	BANDWIDTH_AVAILABLE Bw_remaining	0011000110111	0110001010111	0011011110011
	Channels_available_lo	1111111111111111 1111111111111100	1111111111111111 1111111111111100	1111111111111111 1111111111111110
October 10 18-24 o'clock	BANDWIDTH_AVAILABLE Bw_remaining	0011000110111	1001001110111	0011011110011
	Channels_available_lo	1111111111111111 1111111111111100	1111111111111111 1111111111111101	1111111111111111 1111111111111110
October 11 0-6 o'clock	BANDWIDTH_AVAILABLE Bw_remaining	1001001110111	1001001110111	1001100110011
	Channels_available_lo	1111111111111111 1111111111111101	1111111111111111 1111111111111101	1111111111111111 1111111111111111
October 11 6 o'clock -	BANDWIDTH_AVAILABLE Bw_remaining	1001100110011	1001100110011	1001100110011
	Channels_available_lo	1111111111111111 1111111111111111	1111111111111111 1111111111111111	1111111111111111 1111111111111111

Fig. 9

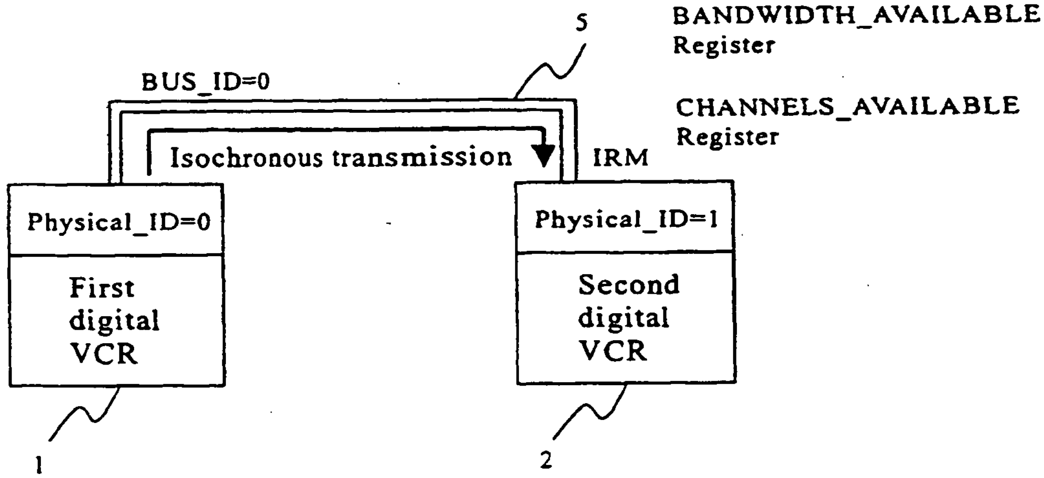

5
BANDWIDTH_AVAILABLE
Register
BUS_ID=0
CHANNELS_AVAILABLE
Register
Isochronous transmission
IRM
Physical_ID=0
First
digital
VCR
Physical_ID=1
Second
digital
VCR
1
2

Fig. 10

Definition

Reservation	bw_remaining
19	13

Initial value

0000000000000000000	1001100110011

BANDWIDTH_AVAILABLE Register

Fig. 11

Definition

channels_available_hi
32
channels_available_lo
32

Initial value

11111111111111111111111111111111
32
11111111111111111111111111111111
32

CHANNELS_AVAILABLE Register

Fig. 12

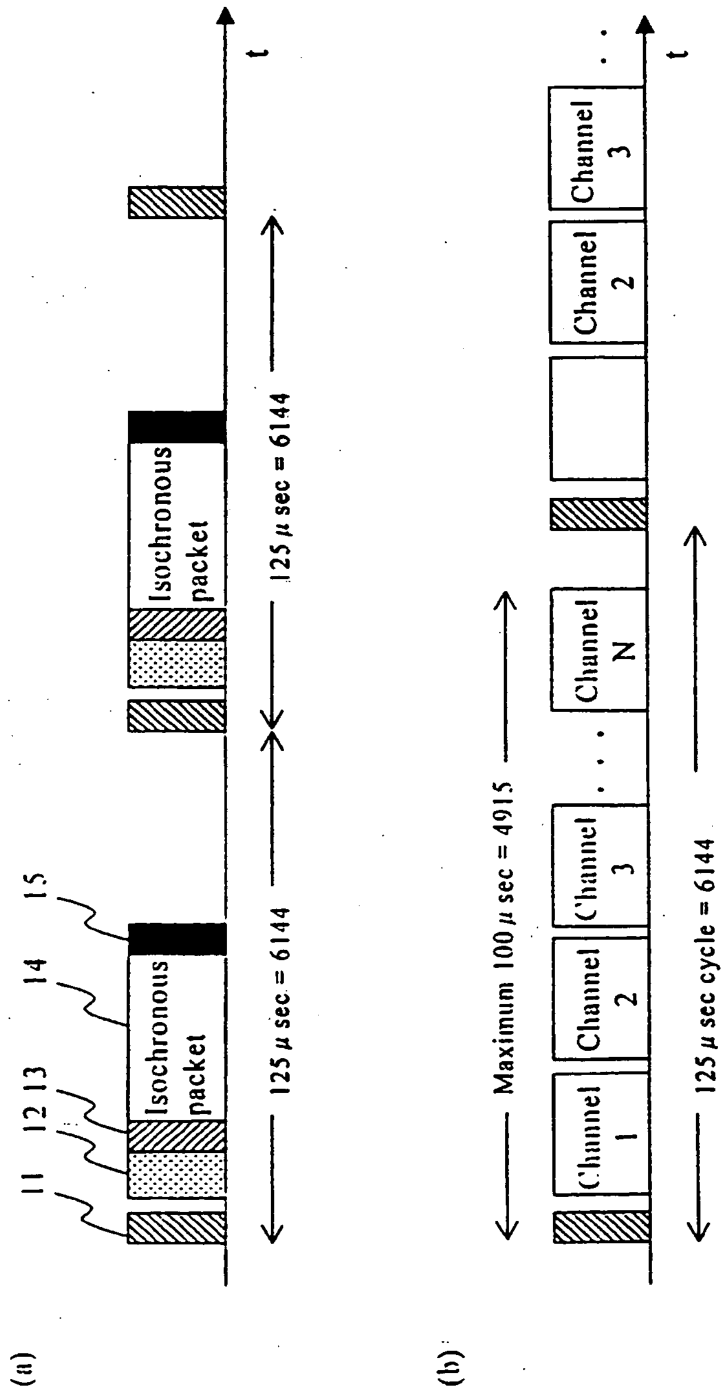

(a)
11
12 13
14
15
Isochronous packet
Isochronous packet
125 μ sec = 6144
125 μ sec = 6144
t
(b)
Maximum 100 μ sec = 4915
Channel 1
Channel 2
Channel 3
Channel N
Channel 2
Channel 3
125 μ sec cycle = 6144
t

Fig. 13

Definition

second_count_hi	second_count_lo
25	7

BUS_TIME Register

Fig. 14

Definition

BUS_ID	Physical_ID	Request_channel _number	Request_bw
start_second_count_hi			start_second_count_lo
end_second_count_hi			end_second_count_lo

TIME_SCHEDULE Register

Fig. 15

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European Patent Office
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(71) Applicant: **Matsushita Electric Industrial Co., Ltd.**
Kadoma-shi, Osaka-fu, 571-8501 (JP)

(72) Inventors:
- **Hamamoto, Yasuo**
  Sakai-shi, Osaka 591-8004 (JP)
- **Takeda, Hidetoshi**
  Neyagawa-shi, Osaka 572-0089 (JP)

(74) Representative: **VOSSIUS & PARTNER**
Siebertstrasse 4
81675 München (DE)

(54) Serial bus control apparatus

(57) Conventional serial bus of IEEE 1394 can not manage a transmission bandwidth and transmission channel for a future time. Therefore, it is not possible to make a reservation for recording from a STB to a VCR connected to the bus. The present invention makes it possible to perform a reservation management of the bus by defining and utilizing registers on CSR space for managing reservations of transmission bandwidth and transmission channel from present time to a future time.

In order to achieve the objects, a serial bus control apparatus of the present invention includes a means for providing a table for controlling a serial bus which has a function for securing a transmission bandwidth for the packet to the serial bus. The table is a reservation control table at least indicating a reservation of a transmission bandwidth and a transmission channel which is required from time T1 until time T2, the reservation control table is stored and controlled on a first register assigned to an address space which is accessible for reading and writing from an arbitrary node on the serial bus. The serial bus control apparatus of the present invention preferably includes a first detection part to detect that the present time is the time T1, the time T2, or the time between T1 and T2. Moreover, the serial bus control apparatus of the present invention preferably includes a rewriting part for rewriting a second register and a third register assigned to a particular address space for a particular node on the serial bus, which second register indicates the available transmission bandwidth at present time and which third register indicates the utilization status of the transmission channel at present time. The particular node on the serial bus is a node, which belongs to the serial bus control apparatus, and a node which includes the second register and the third register control apparatus of the present invention. The serial bus control apparatus of the present invention preferably includes a register providing part for providing a register for reservation control table which table is accessible for reading and writing from an arbitrary node of an arbitrary bus of the N piece of serial buses having the same standard time. In accordance with the present invention, a reservation management for future time using a serial bus for securing the transmission bandwidth and transmission channel according to IEEE 1394 can be achieved, which is not possible with conventional technology. Moreover the serial bus control apparatus of this invention is compatible with conventional systems.

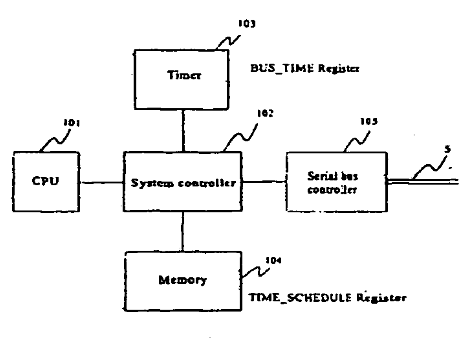

Fig. 1

EP 0 921 472 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 98 12 2576

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X,P	GB 2 317 308 A (KOKUSAI DENSHIN DENWA CO LTD) 18 March 1998 (1998-03-18) * page 3, line 13 - line 28; figure 5 * * page 11, line 16 - page 12, line 24 * ---	1	G06F13/38
Y A	IEEE STANDARDS BOARD: "IEEE Standard for a High Performance Serial Bus" IEEE STANDARD FOR A HIGH PERFORMANCE SERIAL BUS,XX,XX, 1995, pages 199-240, XP002102520 * paragraph '8.1.2! * * paragraph '8.3.1.5! * * paragraph '8.3.2.3.7! * * paragraph '8.3.2.3.8! * * paragraph '8.4.3! * ---	1 2-4	
Y A	US 5 065 393 A (SIBBITT MARCILLE ET AL) 12 November 1991 (1991-11-12) * column 2, line 53 - column 3, line 32; figures 10,12 * * column 3, line 55 - column 4, line 4 * * column 8, line 63 - column 9, line 14 * * column 9, line 39 - line 42 * * column 9, line 54 - line 58 * * claims 1,5 * -----	1 2-4	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 November 2001	Henneman, P

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30-11-2001

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
GB 2317308	A	18-03-1998	JP	10070566 A	10-03-1998
			US	6092113 A	18-07-2000
US 5065393	A	12-11-1991	NONE		

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